REMARKS

I. Present Status of the Application

The abstract of the specification is objected to because it contains legal phraseology such as "comprising". Figure 1 is objected to because of some typing error. Claims 6, 8, 14 and 16 are objected to because of some informalities. The Office Action rejected all presently-pending claims 1-16. Specifically, the Office Action rejected claims 1-4 and 9-12 under 35 U.S.C. 103(a), as being unpatentable over Seal et al. (U.S. 5,583,804). The Office Action further rejected claims 5-8 and 13-16 under 35 U.S.C. 103(a), as being unpatentable over Seal et al. (U.S. 5,583,804), further in view of Morrison et al. (U.S. 6,581,086). In response thereto, Applicants have amended the drawing and abstract to overcome the objections and have amended claims 6, 8, 14 and 16 to improve informalities. After entry of the foregoing amendments, claims 1-16 remain pending in the present application, and reconsideration of those claims is respectfully requested.

II. Discussion of objections

According to the OFFICE ACTION, Figure 1 is objected to because of some typing error. In response thereto, applicants have corrected the label "multiplien" of the reference number "30" into "multiplier." The Abstract of the specification is objected to because it contains legal phraseology such as "comprising". In response thereto, the legal phraseology is deleted

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therefrom. Further, Claims 6, 8, 14 and 16 are objected to because of some informalities. In response thereto, Claims 6, 8, 14 and 16 are amended to overcome the informalities.

Applicants wish to clarify that the foregoing amendments addressed to claims 6, 8, 14 and 16 have been made for purposes of improve informalities in response to the objection of informalities, and not in response to the rejections made based on prior art. Indeed, Applicants submit that no substantive limitations have been added to the claims. Therefore, no prosecution history estoppel arises from these amendments. Black & Decker, Inc. v. Hoover Service Center, 886 F.2d 1285, 1294 n. 13 (Fed. Cir. 1989); Andrew Corp. v. Gabriel Electronics, Inc., 847 F.2d 819 (Fed. Cir. 1988); Hi-Life Products Inc. v. American National Water-Mattress Corp., 842 F.2d 323, 325 (Fed. Cir. 1988); Mannesmann Demag Corp. v. Engineered Metal Products Co., Inc., 793 F.2d 1279, 1284-1285 (Fed. Cir. 1986); Moeller v. Ionetics, Inc., 794 F.2d 653 (Fed. Cir. 1986).

It is believed that the foregoing amendments add no new matter to the present application. Applicants believe that these amendments place the claims in condition for allowance. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

III. Discussion of Office Action Rejection Addressed to Claims 1-4 and 9-12

The Office Action rejected claims 1-4 and 9-12 under 35 U.S.C. 103(a), as being unpatentable over Seal et al. (U.S. 5,583,804, "Seal" hereinafter). Applicants respectfully traverse the rejections for at least the reasons set forth below.

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Independent claims 1 and 9 are allowable for at least the reason that the combination of Seal in view of the alleged well-known art does not disclose, teach, or suggest at least the features of "a special register bank of N-bit data processing registers" and "a selector, coupled to the special register bank and the general register bank, for selecting one of the special and general register banks and outputting a selected N-bit result from the selected register bank, wherein the selected N-bit result and a N-bit data form a 2N-bit addition operand", as claimed in claim 1, and "selecting one of the special and general register banks and outputting a N-bit result from the selected register bank, wherein the N-bit result and a N-bit data form a 2N-bit addition operand", as claimed in claim 9, which are also admitted by the Office Action.

The Office Action alleged that even Seal failed to teach the "special register bank of N-bit data processing registers" and "selector", the general register bank (106 of Fig.1) having only two read ports and taking at least two cycles for a multiply-accumulate instructions to execute (Col.5, Lines 60-64), however, it is well known in the art that reducing the amount of cycles that instructions take to execute is of paramount concern. One of ordinary skill in the art at the time of the invention made would have recognized that placing two register banks with two read ports each allows 4 read ports to be active at once. Therefore, it would have been obvious to one of ordinary skill in the art to combine two general banks in parallel in order to read out twice as many operands in half as much time, reducing the amount of cycles a multiply-accumulate instruction takes to execute. Applicants do not agree with such allegation and further explain as follow.

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A. Seal Different From the Invention

It is well established at law that, for a proper rejection of a claim under 35 U.S.C. §103 as being obvious based upon a combination of references, the cited combination of references must disclose, teach, or suggest, either implicitly or explicitly, all features of the claim at issue.

Seal disclosed a data processing system utilizing a multiplier-accumulator that performs both a first class of multiply-accumulate instructions and a second class of multiply-accumulate instructions. The first class of multiply-accumulate instructions are of the form N*N+N→N and the second class of multiply-accumulate instructions are of the form N*N+2N→2N. The second class of multiply-accumulate instructions provide a greater precision of arithmetic in a single instruction and avoid the use of excessive instruction set space by being constrained that the result is written back into the two registers from which the 2N-bit accumulate value was taken *(See Abstract of Seal)*.

In the architecture of Seal, for a greater precision of arithmetic in a single instruction, the multiplier-accumulator multiply an N-bit operand held in a first data processing register by an N-bit operand held in a second data processing register and add a 2N-bit operand held in a third and a fourth data processing registers to yield a 2N-bit result that is restored in the third and a fourth data processing registers *(Registers R7 and R11, as shown in Fig. 3 of the Seal)*. For a lower precision of arithmetic in a single instruction, the multiplier-accumulator multiply an N-bit operand held in a first data processing register by an N-bit operand held in a second data processing register and add an N-bit operand held in a third data processing register to yield an N-bit result that is stored in a fourth data processing register.

However, in the present invention, as stated in Page 7 of the SPECFICATION, clearly stated if the class of instructions is the first class with a higher precision, for example, the desired calculation is N*N+2N→2N, the class signal causes the selector to provide the 2N bits of the addition signal including the first part C and the second part D, **both of which are from the general register bank to the accumulator**. If the class of instructions is the second class with a lower precision than the former, for example, the desired calculation is N*N+N→N, the class signal causes the selector to provide the 2N bits of the addition signal including the first part C and the second part D. **The first part C is provided by the special register bank and the second part D is provided by the general register bank**. In the case of proceeding with the second class of instructions, the first part C can be used for some other functions as required, for example, detecting overflow conditions after the 2N-bit multiplied result from the multiplier being added with the addition operand (including the first part C and the second part D).

Seal failed to disclose, teach, or suggest, either implicitly or explicitly the "special register bank of N-bit data processing registers" and "selector", as claimed in claim 1, and "selecting one of the special and general register banks and outputting a N-bit result from the selected register bank, wherein the N-bit result and a N-bit data form a 2N-bit addition operand", as claimed in claim 9. Thus, the apparatus and method for processing data as claimed in claims 1 and 9 are totally different from that of the Seal.

B. The Well-Known Art Does Not remedy the deficiency of the Seal

Applicants **do no agree with** the allegation in the Office Action stating that "the general register bank (106 of Fig.1) having only two read ports and taking at least two cycles for a

multiply-accumulate instructions to execute (Col.5, Lines 60-64), however, it is well known in the art that reducing the amount of cycles that instructions take to execute is of paramount concern. One of ordinary skill in the art at the time of the invention made would have recognized that placing two register banks with two read ports each allows 4 read ports to be active at once."

In the architecture of **Seal**, please refer to Fig. 2, if the first class of multiply-accumulate instructions of the form N*N+N→N are performed, registers R0, R2, R5 are used to store the operands and register R10 is used to store the result. Please also refer to Fig.3, if the second class of multiply-accumulate instructions of the form N*N+2N→2N are performed, registers R1, R2, R7 and R10 are used to store the operands and the result is restored to registers R7 and R10.

If the architecture of **Seal** is combined with the well-know art "placing two register banks with two read ports each allows 4 read ports to be active at once" as alleged in the Office Action, according to the disclosure upon which the Office Action relied (Col.5, Lines 60-64), it was stated, "the processor core 102 that is illustrated in FIG. 1 performs two cycles of initialization, reading two registers one each cycle. **This is a result of having only two read ports to the register bank 106**." That is, even combined with the alleged well-known art, adding additional register bank just can achieve **One cycle of the initialization**. Actually, the combination of **Seal** and the alleged well-known art still failed to disclose, teach, or suggest, either implicitly or explicitly the "special register bank of N-bit data processing registers" and "selector", as claimed in claim 1, and "selecting one of the special and general register banks and outputting a N-bit result from the selected register bank, wherein the N-bit result and a N-bit data form a 2N-bit addition operand", as claimed in claim 9.

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Consequently, the combination of Seal and the alleged well-known art does not render claims 1 and 9 obvious, and the rejection should be withdrawn.

Because independent claims 1 and 9 is allowable over the prior art of record, their respective dependent claims 2-4 and 10-12 are allowable as a matter of law, for at least the reason that these dependent claims contain all features of their respective independent claims 1 and 9. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). Additionally and notwithstanding the foregoing allowability of these dependent claims, the dependent claims recite further features and/or combinations of features that are patentably distinct from the prior art of record. For example, dependent claim 3 further recites "the selector further receiving a class signal, wherein the selector selects one of the special and general register banks in response to the class signal."

IV. Discussion of Office Action Rejection Addressed to Claims 5-8 and 13-16

The Office Action further rejected claims 5-8 and 13-16 under 35 U.S.C. 103(a), as being unpatentable over Seal et al. (U.S. 5,583,804), further in view of Morrison et al. (U.S. 6,581,086). Applicants respectfully traverse the rejections for at least the reasons set forth below.

Because independent claims 1 and 9 is allowable over the prior art of record, their respective dependent claims 5-8 and 13-16 are allowable as a matter of law, for at least the reason that these dependent claims contain all features of their respective independent claims 1 and 9. Additionally and notwithstanding the foregoing allowability of these dependent claims, the dependent claims recite further features and/or combinations of features that are patentably distinct from the prior art of record. For example, dependent claim 5 further recites "a detecting

device, coupled to the accumulator, for receiving the 2N-bit accumulated result and for checking if a case of overflow occurs." Depend claim 13 further recites "a step of receiving the 2N-bit accumulated result and checking if a case of overflow occurs."

The Morrison Does Not remedy the deficiency of the Seal

In the Office Action, **Morrison** is cited to remedy the deficiency of the **Seal**. As alleged by the Examiner, according to the disclosure of the **Morrison**, one of the ordinary skill in the art would have recognized that overflow detection is desirable in order to prevent errors from propagating through a data processing system without having to recalculate operations already performed. Therefore, one of ordinary skill in the art at the time of the invention would have found it is obvious to include a comparator connected to the accumulator to detect overflow to prevent error propagation.

Applicants **do no agree with** the allegations. The disclosure, upon which the Office Action relied, Col. 9, Lines 24-42 in **Morrison**, stated,

> The output of the priority encoder is provided to the comparator, which **compares the location of the first bit value change with the location of the selected bits** to determine if there is an overflow. If there is no overflow, the comparator controls the selection of the MUX to output the selected subset of bits. On an overflow, the comparator controls the selection MUX to output a saturated value.

The overflow condition disclosed in the Morrison is the location of the first bit value change with the location of the selected bits, which is totally different from the overflow detection as claimed in the invention.

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As stated above, in the invention, if the class of instructions with a lower precision is performed, the class signal causes the selector to provide the 2N bits of the addition signal including the first part C and the second part D. **The first part C is provided by the special register bank and the second part D is provided by the general register bank**. As stated in Page 9, Lines 12-16, it states "the detection device 170 will compare the first N-bit part **H** of the accumulated result 154 with the first N-bit part **C** of the addition operand 152, which is supplied by the special register bank 110. If the first N-bit part **H** of the accumulated result 154 is not the same as the first N-bit part **C** of the addition operand 152, it means that an overflow case is occurred in this calculation."

Furthermore, even the **Seal** is combined with the disclosure of the **Morrison**, the Seal does not still disclose, teach, or suggest, either implicitly or explicitly, "a detecting device, coupled to the accumulator, for receiving the 2N-bit accumulated result and for checking if a case of overflow occurs" as claimed in claim 5 and "a step of receiving the 2N-bit accumulated result and checking if a case of overflow occurs" as claimed in claim 13. The deficiency of the Seal is still not remedied and the combination thereof can not render the claims 5 and 13 obvious.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-16 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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